REMARKS

The undersigned attorney is grateful to the Examiner for the detailed and helpful Office Action.

Claims 11-13 are in the case.

In an Office Action dated July 22, 2003, the following requirements and objections to the specification and drawings were made: A new title is required; the abstract is objected to; and a proposed drawing correction is required.

In the same Office Action claims 11-13 were rejected. Claims 11-13 stand rejected under 35 U.S.C. 112, second paragraph as being indefinite. Claims 11 and 12 stand rejected under 35 U.S.C. 103(a) as being obvious in light of the applicant's admitted prior art in view of Buch. Claim 13 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Buch in view of Chiang et al.

The requirements have, it is believed, been satisfied by the above amendments. The Abstract has been amended by the above amendment.

With respect to the suggestions for amending the claims, the claims heave been amended to overcome the Examiner's basis for the suggestions except the suggestion to delete lines 23-27. Lines 23-27 do not seem to be repetitive of lines 18-22.

The rejections under 35 U.S.C. 112, second paragraph, have been, it is believed, obviated in the new claims.

With respect to the rejection of claim 11 under 35 U.S.C. 103(a) it is not obvious that the combination of the applicant's admitted prior art in view of Buch would lead one to the present invention. It is clear that at some noise level the hold circuit of Buch would fail, such as if lighting struck the circuit or ionizing radiation of sufficient magnitude was present at the circuit board.

The hold circuit of Buch and of Figure 2 of the present invention is more susceptible to noise when it is holding the data on the data lines by itself. That is because the effective output impedance of the circuit 220 is higher than for the amplifiers and gates driving the data lines. For example, if a data line is at a logical 0 (zero voltage) and at some time an amplifier or gate tries to drive the data line to a logical one (a high voltage such as 5 volts), the resistor 12 must be large enough so that a sufficient voltage is generated across the resistor when the data line is being driven by the amplifier or gate to provide a high enough voltage to guarantee that the amplifier 10 will switch from a logical zero output to a logical one output. Thus, there is a lower limit to resistance of resistor 12, and the combination of the amplifier 10 and resistor 12 provides an effectively higher output impedance than an amplifier or gate by itself. If the noise gets too high, the hold circuit will not be able to hold the data lines at a zero or

one logic level while amplifiers and gates driving the data lines, because of their lower effective output impedance, would be able to hold the logic level constant. It is not obvious that the threshold level of noise generated in a passenger railway car is below this threshold level.

If, at any time, the Examiner in charge of this application feels that prosecution of this application could be expedited through a telephone interview, the Examiner is invited to contact the undersigned by telephone at (412) 380-0725.

Respectfully Submitted,

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~~PROGRAMMABLE SYSTEM INCLUDING SELF LOCKING MEMORY CIRCUIT FOR A~~

PASSENGER TRANSIT CAR INCLUDING A SELF-LOCKING MEMORY

OR BUS CIRCUIT FOR A TRISTATE DATA BUS

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(e) from Provisional Application Serial No. 60/109,951, filed on November 25, 1998 and entitled "Intelligent Door Controller Unit". This Provisional Application is assigned to Westinghouse Air Brake Company, the assignee of the present application, and is incorporated herein by reference thereto.

FIELD OF THE INVENTION

The present invention relates, in general, to memory circuits and, more particularly, this invention relates to the details of a simple, self-locking memory circuit for a tristate bit line of a data bus.

BACKGROUND OF THE INVENTION

In the above-noted provisional application, a self-locking circuit is shown connected to a tristate bit line of a data bus interconnecting a central processing unit (or "CPU") and other digital transceiving processing devices, such as a Motion Control Digital Signal Processor (or "DSP"), to provide a memory of the

last data value or electrical potential sent on such line, i.e., the last read or write transfer between the CPU and the processing devices. The line is said to be "tristate" because of the three voltage states which the line can assume, namely, a high voltage state, a low voltage state and a state in which no current flow is generated.

The self-locking circuit of the invention is useful on any connecting bit line where it is desirable to latch and hold the last value or state on the line and thereby retain and maintain such value once the driver relinquishes control of the line, i.e., when the line returns to a high impedance state.

SUMMARY OF INVENTION

The present invention uses a known, commercially available, non-inverting, non-clocking buffer amplifier chip and a simple parallel resistor connected across the chip, i.e., connected to the input and output terminals of gates of the chip. These two means (chip and resistor) when connected to a tristate bit line provide a predetermined relatively high impedance on the line that is effective in latching the latest value found on the line.

More particularly, a circuit device supplying the bit line with a signal has a relatively low impedance. The relatively low impendence of the supply device and the relatively high impedance of the latching circuit of the invention provides a voltage divider

that produces a low voltage at the supply circuit while the high impedance of the latching circuit develops a relatively high voltage.

When the signal from the supply device or circuit goes from a low state to a high state, the output voltage of the latching circuit is at a low state. Thus, the input voltage to the amplifier chip and resistor of the latching circuit of the invention initially rises to the voltage divided level. At a certain voltage threshold, the latching circuit switches to the high state, with the output terminal of the chip now also being in a high state. The latching circuit now has essentially the same high state as the output of the supplying (or sending) circuit.

Since the chip has no clocking elements, it is stable over time and holds the value received from the sending circuit. It will not switch until such time as a new value is imposed on the input terminal of the latching circuit at a level that moves through a low voltage threshold value to return the circuit to a low state. Again, the circuit will hold this "low" value until it is forced to change by a new "high" state sent on the bit line and imposed upon the latching circuit.

In the above incorporated provisional patent application, for example, the timing structures of the CPU and DSP are different. By holding data over time, the circuit of the present invention

allows the CPU and DSP to work together while simultaneously preventing noise on the bit line from being transferred between the CPU and DSP, i.e., the impedance of the circuit of the invention temporarily changes (lowers) only when the latest value or state on the bit line builds or lowers to a current level above or below the threshold levels of the circuit, after which the chip of the circuit conducts. When this occurs, the impedance of the circuit temporarily falls to a low value, temporarily loads the line, then returns to the relative high impedance value to hold the new, latest value and to remove the load from the line. In this manner, the circuit is self-locking and resists transferring noise and electromagnetic interference, as such noise and interference do not sustain current levels sufficient to force the switching of the circuit.

OBJECTS OF THE INVENTION

It is, therefore, one of the primary objects of the present invention to provide a simple digital latching circuit for retaining the latest information (high or low state) conveyed on a bit line.

Another object of the present invention is to provide a data latching circuit that requires no clocking, timing or synchronization pulses to latch the data.

Yet another object of the present invention is to provide a means for testing the integrity of a printed circuit board bus signal.

Still another object of the present invention is to use a commercially available, non-inverting digital amplifier chip and an electrical resistor connected across the chip as the latching circuit of the invention, with the chip and resistor providing a predetermined impedance for such latching circuit.

A further object of the present invention is to provide a digital circuit having the capability of extending the hold times of data conveyed on bit lines connected between digital circuit devices.

Yet another object of the present invention is to provide a circuit that exhibits a substantial reduction in noise and interference for tristate digital bit lines.

In addition to the specific objects and advantages of the present invention described above, various other objects and advantages of the invention will become more readily apparent to those persons who are skilled in the relevant memory circuit art from the following more detailed description of the invention, particularly when such description is taken in conjunction with the attached drawing Figures and with the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B, taken together, present a schematic diagram showing eight buffer memory latching circuits of a presently preferred embodiment of the invention and their connection to the bit lines of an eight bit data bus;

Figure 2 is a circuit diagram useful in explaining the operation of the presently preferred embodiment of the latching circuit of the present invention;

Figure 3~~A~~ illustrates a typical passenger transit train including the central door controller (CDC) in the lead railcar, the door controller units (DCUs) on each railcar to which the CDC is linked, and the door operator(s) which each DCU drives;

~~Figure 3B is a perspective view of one type of door operator installed over a doorway whose doors are shown open;~~

~~Figure 3C is a perspective view of the door operator of Figure 2 with the doors shown closed over the doorway;~~

Figure 4 is a simple block diagram of an intelligent door controller unit (IDCU) according to the invention.

Figure~~s 5A-B~~ 5 illustrate~~s~~ an expanded version of the block diagram of Figure 4 showing a preferred modular architecture for the IDCU inclusive of a CPU card, a power supply card, and a motor driver & input/output (MD-I/O) card~~,~~.

~~Figure 6 illustrates a basic configuration for the IDCU in which a single IDCU is used to control each doorway;~~

~~Figure 7 illustrates an advanced configuration for the IDCU in which a single CPU card can support multiple MD-I/O cards to control multiple doorways;~~

~~Figures 8A-C illustrate a circuit layout for the MD-I/O card shown in Figures 5A-B inclusive of a mirror-image optoisolator device, complex programmable logic devices (CPLDs), a motion control processor and an H-bridge amplifier;~~

~~Figure 9 is a schematic of a mirror-image optoisolator circuit and the two mirror-image registers to which it writes in the input/output (I/O) CPLD on the MD-I/O card;~~

~~Figures 10A-C illustrate one possible scheme for the I/O-CPLD and related circuits on the MD-I/O card;~~

~~Figure 11 illustrates one possible scheme for the address (ADD) CPLD and related circuits on the MD-I/O card; and~~

~~Figures 12A-E illustrate one possible scheme for the motor control (MC) CPLD and related circuits on the MD-I/O card.~~

BRIEF DESCRIPTION OF A PRESENTLY PREFERRED EMBODIMENT

Reference is now made, more particularly, to the drawings. Figures 1A and 1B together show eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tristate bit lines 0 through 7 of a data bus 9 interconnected between transceiving digital components 20 and 30. An example of such an interconnection of components is the central processing unit (or "CPU") 230, the Motion Control Digital Signal Processor (or "DSP") 320 and the Complex Programmable Logic Device (or "CPLD") 300 interconnected in the read/write manner shown in Figures 5B and 8B of the above incorporated provisional patent application.

The buffer memory circuit of the invention bears the same reference numeral (220) found in the above provisional application.

The buffer memory of the present invention, however, has utility on any data bus or digital circuit where memory of the last transfer of data requires retention and can be used on any number of bit lines.

The eight circuits 220 which are illustrated in Figures 1A and 1B are substantially identical so that only one of the circuits is discussed herein in detail. This circuit is shown, in Figure 2 of the drawings, connected to a bit line 4 extending between the two digital circuits 20 and 30.

More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level for circuit 220.

The circuit operates in the following manner:

The input to circuit 220, in Figure 2, is received from a digital circuit device represented schematically by an amplifier

symbol 20 and a resistor 22. Resistor 22 represents the internal output impedance of amplifier 20 and is determinative of its output voltage. The electrical output impedance of amplifier 20 is relatively low in comparison to that of resistor 12 of latching circuit 220 such that any voltage developed by amplifier 20 divides at the connection 24 of the two resistors 22 and 12, with the greater of the two voltages being developed across resistor 12.

For example, if amplifier 20 produces a five volt signal, it can divide on a one and four volt basis, with the four volts being applied to the input terminal 14 of chip 10. The present state of chip 10, however, may be at zero volts, i.e., zero volts at its input and output terminals 14 and 16. Output terminal 16 and a series resistor 26, which represents the internal impedance of chip 10, are a virtual ground or virtual Vcc for circuit 220. Resistances 12 and 26 represent the total impedance of circuit 220 of the invention.

In the case of amplifier 30, as schematically presented, a resistor 32 is shown in Figure 2 that represents the internal impedance of the amplifier 30.

Circuit 220 has a voltage threshold level that permits the circuit to change states. If the divided voltage is at the threshold level, circuit 220 switches to a state where its input and output terminals 14 and 16 are now at a "high" state, such as

the above divided four volt level. This occurs by chip 10 momentarily conducting, thereby momentarily loading the bit line, bit line 4, for example. As soon as the chip 10 conducts and goes "high", conduction and loading of the bit line 4 ceases. Being a non-inverting device, chip 10 does not change the state or potential of the latest signal applied thereto.

In the drawing figures, amplifier symbol 20 is shown as a tristate bus driver but it is also a tristate receiver, as indicated by a second amplifier symbol 20A. The third amplifier (symbol 30) is also a bus receiver and driver, the dual function being again indicated by a second amplifier symbol 30A. In the read/write arrangement of the CPU and DSP in the above noted provisional application, the driver/receiver functions are interchangeable such that amplifier 30 can be the driver and amplifier 20 the receiver. In either case, circuit 220 holds the latest potential supplied on the bit line until one of the two, upper and/or lower thresholds of circuit 220 are crossed.

In crossing the lower threshold of circuit 220, amplifier 20 or 30 will place a "low" potential on the bit line while the other circuit is in a high state. Circuit 220, which is presently latched in a high state, tries to maintain the high state. However, when the voltage on input terminal 14 of chip 10 drops through the low threshold before the chip 10 conducts and switches

to the low state, the chip 10 temporarily and momentarily loads the bit line 4. As the output 16 of the chip 10 changes state, the chip 10 immediately thereafter ceases conducting, unloads the bit line 4 and holds the new "low" state until such time that its upper threshold is reached, which occurs when a "high" voltage is received at input terminal 14.

Circuit 220 loads the bit line only when it switches (i.e. when chip 10 conducts) which makes the circuit 220 highly effective in resisting electromagnetic noise and interference, as such noise and interference can not sustain current flow and a voltage level sufficient to reach the switching thresholds of the circuit 220.

Further, the circuit 220 does not oscillate, as there is no phase shift between the input 14 and output 16 of chip 10. The circuit 220 is a digital device having only high and low states. The circuit 220 latches and locks itself until its thresholds, high and low, are reached by a new state on the bit line.

In this manner, circuit 220 retains the latest information until it is forced to change, as per above. If the circuit 220 does not retain the last bit of information (potential), it is an indication of current leakage on the circuit board (not shown) on which chip 10 and resistor 12 are mounted. Circuit 220 thereby provides, in addition, an internal diagnostic function on the

board. It alerts a technician of such a problem so that he or she can proceed to find the location of the leakage.

Because the circuit 220 extends hold times of data, it functions to match the timing of respective devices interconnected by bit lines that transfer data, such as the amplifiers 20 and 30, or the CPU and DSP devices described in the above incorporated provisional patent application and described below. As noted above, the CPU and DSP do not have a one hundred percent match in their timing requirements.

The following background information is provided to assist the reader to understand the environment in which the invention will be used. The terms used herein are therefore not intended to be limited to any particular narrow interpretation unless specifically stated otherwise in this document.

Shown in Figure 3~~A~~ is a typical passenger transit train. It has a lead railcar 41 and a plurality of trailing railcars 41 each linked serially by means of a mechanical coupler. Various electrical trainlines 130 span the length of the train. Each trainline is composed of a series of interconnected wires, with each such wire contained (along with the wires of the other trainlines) within a protective conduit secured to the underside of each railcar. Each such conduit connects via an electrical connector 132 to another such conduit on a neighboring railcar so

as to extend each trainline along the train. These trainlines are used to carry the electrical signals that are needed to operate and control the various systems on each of the railcars in the train.

Like the lead railcar, each of the trailing railcars may be equipped with one or more motors and a propulsion controller unit with which to control them.

Each transit railcar has one or more openings or doorways 37 through which passengers can enter and exit the railcar. Over each doorway 37 is installed a door hardware system (DHS), also referred to as a door operator 40, to which the door panel(s) attach. The door operator is what actually moves the door panel(s) back and forth over the doorway to open and close the doors, depending on whether its motor is commanded to rotate in the opening or closing direction.

In addition to the propulsion motors, the doors of the railcars in a passenger train are also centrally controlled from the lead railcar. Specifically, a central door controller (CDC) 33 housed in the lead railcar communicates with, and controls, one or more door controller units (DCU) 74 on each railcar through a number of discrete door control trainlines 130. Each DCU 74 controls one or more door operators 40, and their associated motors.

Specifically, each door operator 40 is deployed with one or more door lock solenoids 34 and a side select emergency lockout solenoid 36, both controllable by the DCU 74 in response to the side select signal. Additional outputs are the lock 38 and unlock 40 for the cliff/side lockout, a close confirmation interlock solenoid 42 and a warning lamp/fault indicator 44.

The local door hardware signals that the DCU 74 receives typically come from switches that are used to sense the status of the doors. Such door status switches are typically part of the door operator assembly 40, though they may also be added to the door hardware subsequently. Most of these switches have two contacts, the first contact of each switch being used to provide an input to the DCU 74. Each switch is dedicated to sensing whether or not a particular part of the door operator/DHS 40 has assumed a given state.

A cliff side select trainline is used by many transit authorities to selectively disable (i.e., physically lockout) the INT EMER door release handles on one or both sides of the train. Each lockout assembly includes a bi-stable relay, a movable plunger and a locking pin connected to the plunger.

~~Among the many door operators to which the invention(s) disclosed herein is directed is the door hardware system 35 disclosed in the text and figures of U.S. Patent Application Serial~~

No. 09/099,260, now US Patent 6,032,416. For the sake of clarity, the reference numerals used to denote the door operator hardware herein are the same as those used in the cited document. Figure 3B shows an opening 37 in a sidewall 39 of a railcar 41. Fixed to or incorporated as part of the body of railcar 41 above opening 37 is a base plate 34 disposed just above and horizontally along the length of opening 37. It is to this base plate 34 that the door hardware system 35 attaches to railcar 41.

The first and second door lock assemblies 44 and 117, as well as motor 76, are attached to the base plate 34 of railcar 41 by means of bolts and brackets. Specifically, motor 76 is bolted to the base plate via an L-shaped bracket. The first door lock assembly 44 is bracketed to base plate 34 above the left vertical edge of opening 37. Similarly, the second door lock assembly 117 is bracketed to base plate 34 above the right vertical edge of opening 37.

Viewed from left to right in Figures 3B and 3C, the drive mechanism 170 includes coupling 77, drive shaft 78, coupling 81, first helical screw 80, center coupling 104, second helical screw 102, and first and second drive nut assemblies 150 and 190, respectively. Controlled by a DCU based on various central command signals and local door hardware signals, the motor 76, and the gear

~~reducer unit 79 at its right to which it is connected, is what drives the drive mechanism 170.~~

Illustrated in Figures 4 ~~through 12~~and 5 are the essential details of an intelligent door controller unit (IDCU) and related inventions. The IDCU is preferably organized into three modules: a CPU card 200, a motor driver & input/output (MD-I/O) card 300, and a power supply card 400~~, as best shown in Figures 4 and 5A-B~~. Each of these cards features a printed circuit board onto which an industry-standard bus structure, such as the PC-104 embedded processor interface, has been laid out. A simplified representation of the bus structure is shown in Figures ~~5A-B, with a more detailed depiction shown in Figures 8A-C~~ 5. It is into this bus structure that the addressable components of the invention have been incorporated.

Designed to serve as the motherboard for the IDCU, the MD-I/O card 300 has upwardly disposed connectors built into its bus structure. Being physically linked to the motherboard via such connectors, the CPU and power supply cards 200 and 400 can thus be stacked horizontally atop the MD-I/O card 300. This allows the IDCU to be contained compactly within a single enclosure. As explained in greater detail below, this modular architecture also allows more capability to be added to the IDCU merely by connecting

additional cards to the vertical bus structure by which the desired functions can be implemented.

The CPU card 200 includes a standard serial port 210, the databus memory buffer circuitry 220, and a microprocessor 230 accompanied by the appropriate volatile and non-volatile memories to store data and programming code and by various complex programmable logic devices (CPLDs) to perform CPU-type functions such as address decoding and buffering.

As best shown in Figures ~~5A-B~~4 and ~~8A-C~~, among other components, the MD-I/O card 300 includes a novel optoisolator device 310, several CPLDs, a motion control (digital signal) processor 320 (DSP chip), an H-bridge amplifier 330, a seven segment display 340, and a tone/audio amplifier 350. Three CPLDs are critical to the operation of the MD-I/O card 300: the ADD-CPLD~~,~~ ~~the I/O-CPLD~~ 316, the I/O-CPLD including two separate blocks in Figure 4, an I/O input 312 and as I/O output 314, and the MC-CPLD 318. The ADD-CPLD 316 handles the address decoding functions. The I/O-CPLD handles the input and output functions of the IDCU. The MC-CPLD 318, in conjunction with the DSP chip 320, handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door operator. These CPLDs are preferably in-system-programmable (ISP) devices. Well known in the electronic arts, each CPLD is capable of being

programmed/reprogrammed within the bus structure of the circuit into which it has been incorporated. Each CPLD also features in-system diagnostic capabilities, meaning that each is capable of storing data about its own operations and reporting such data to the CPU card 200 when queried for same as part of the diagnostic tests.

~~The ADD-CPLD is incorporated into the bus structure as shown in Figure 8B. It can take the form of an ISP version of the industry standard GAL 22v10, such as the one manufactured by the Lattice Semiconductor Corporation. The address decoder chip monitors the addresses that are issued by the CPU. Should the CPU fail in such a way that it issues addresses outside a predetermined range, the ADD-CPLD will cause the MC-CPLD to shutdown in a safe manner and, optionally, cause the warning lamp outside the affected doorway to flash. Likewise, the CPU monitors the address and data buses for erroneous conditions or faulty data issued by any of the CPLDs or the motion control processor. Should the CPU detect such errors, it can likewise cause a safe shutdown of the IDCU.~~

~~An important feature of the address decoder chip is that it can be reprogrammed at any time to support different address groups. This feature allows multiple MD-I/O cards to be connected off of one CPU card 200. An example of the logic programmed into the ADD-CPLD is illustrated in Figure 11.~~

~~As an address decoder, the function of the ADD-CPLD is relatively simple in that it has only to produce six address strobe pulses for the address bus on the MD-I/O card. Each of the address strobes is configured to cover two address locations, each giving a total addressing range of twelve bytes. The starting address location was tentatively set at 300 (hex), as it is relatively unused by other PC devices. Considering that the design is based on an ISP chip, the addressing can be changed at any time as conditions dictate. To be compliant with the IBM PC I/O specification, only sixteen of the twenty four I/O address lines are decoded, the remaining eight lines will produce 256 echo locations throughout the memory map of the IDCU.~~

The I/O CPLD 312, 314 is the component through which the central command signals and the local door hardware signals are input into the IDCU. As can be seen from Figures 4~~, 5A-B,~~ and ~~8A-C~~5, the I/O-CPLD 312, 314 chip serves as the interface between the main control components of the IDCU and the CDC of the transit authority. The I/O-CPLD 312, 314 can take the form of the ISP-2064 chip manufactured by the Lattice Semiconductor Corporation. The IO CPLD block 314 has connected to it an IO output over current protection circuit 370.

The I/O CPLD 312, 314 is preferably deployed with the novel optoisolator device 310, also referred herein as the mirror-image

optoisolator circuitry. It is well known, of course, that all of the central command inputs are considered extremely safety critical because a fault anywhere in the input path that these signals follow into a DCU can cause given rise to serious problems within any door system. The I/O-CPLD 312, 314 and the optoisolator device 310 together serve to monitor and verify the central command signals that the IDCU receives from the CDC.

As noted earlier, the IDCU can accept central command signals from either the discrete trainlines 130 (i.e., a hard-wired switch interface) or an optional serial communications link 328. For example, regarding the discrete trainlines 130, the central command inputs can be conveyed to the IDCU via a single-switched or a doubled-switched input format. In the single-switched format, one line is activated and its associated return line (commonly the ground) is hardwired to the CDC. In the doubled-switched format, both the input line and its associated return are activated together at the CDC. When not in use, both lines are shorted together to reduce the chance of unwanted bias voltages or ground loops from triggering a door control signal.

The optoisolator device 310 optically isolates the IDCU from the discrete trainlines whether conveyed via the single-switched or the doubled-switched input format. It is well known that the discrete trainlines are susceptible to picking up rather high

voltage spikes from the environment in which they are used. Transit authorities thus require optical isolation because it protects the IDCU from such high voltage spikes; spikes that could otherwise cause the doors to operate improperly and even damage the electronics. Once the central command inputs are received by the optoisolator device 310, they are clamped and filtered~~, as best shown in Figure 9,~~ to reduce the possibility of transients from getting into the IDCU via the I/O-CPLD 312, 314. For each input line, an input-voltage decoupler is used to minimize the effects of low-voltage DC bias signals. In addition, the values of the input circuits are tailored to suit the voltage requirements of the train. Furthermore, the line filters are tuned to minimize the electrical noise spectrum expected to be seen by the IDCU.

In addition to monitoring and verifying the authenticity of all trainline inputs, the CPU 200 and I/O-CPLD 312, 314 together route the incoming central command inputs and local door hardware inputs to the appropriate component in the IDCU so that the required task(s) can be performed. The I/O-CPLD 312, 314 is also programmed to handle various output functions for the IDCU. The following is merely a brief list of the functions that the I/O-CPLD 312, 314 can be programmed to perform: filter the central command signals received from the trainlines; monitor and decode all central command inputs; detect erroneous signals; generate CPU I/O

interrupt signals; monitor various passenger activated switches; control speaker/beepers on MD-I/O card 300; control the warning lamp(s) outside the doorway(s); monitor power-supply voltages; monitor the I/O output fault status; test the optocouplers; test the input and encoder connectors for proper connection; transfer status and interrupt data to the MC-CPLD 318; generate the clock pre-scalar signals; and control one of the two unlock actuators ~~49 or 113~~ of the two door ~~lock assemblies 44 and 117. An example of the logic programmed into the I/O-CPLD is illustrated in Figures 10A-C~~37 lock assemblies.

Referring now to Figures 4~~, 5A-B~~ and ~~8A-C~~5, the MC-CPLD 316, in conjunction with the motion control processor (DSP chip) 320, handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door operator. The MC-CPLD 318 and the DSP chip 320 can take the form of the ISP-1032 and LM629 chips manufactured by the Lattice Semiconductor Corporation and National Semiconductor Corporation, respectively. Like the aforementioned CPLDs, these chips are commercially available devices. The following specification sheets for these devices are incorporated herein by reference: ADD-CPLD (ISP22lv_03 sheet dated March 1998), I/O-CPLD (2064_04 sheet dated October 1998) and MC-CPLD (1032_05 sheet dated October 1998) published by Lattice Semiconductor Corporation; and the LM629 chip (TL/H/9219

dated February 1995) published by the National Semiconductor Corporation.

The MC-CPLD and various related circuits and components are disposed on the MD-I/O card 300~~ as shown in Figures 12A-E~~. The output control circuits in the MC-CPLD 316, as well as those in the I/O-CPLD 312, 314, have built-in short circuit protection, which will shutdown the output operations should a fault be detected. Implemented primarily within the MC-CPLD chip 316 are the data/address control logic~~ as shown in Figure 12A~~, the current feedback and deadtime circuitry~~ shown in Figure 12B~~, the encoder monitoring circuitry~~ shown in Figure 12C~~, and the interrupt control logic~~ shown in Figure 10E~~. The access key circuitry 322, the watchdog timer circuitry 324 and the motor control circuitry for the H-bridge 230, shown in Figures 4~~, 5B~~ and ~~12D~~5, are implemented both internal and external to the MC-CPLD. The integration capacitor circuitry 325 is external to the MC-CPLD 318, as is best shown in Figure 5~~B~~. This circuitry is used to monitor the power/wattage in the motor 76 during overload conditions, otherwise it is discharged.

Regarding the motion control processor 320, the LM629 chip was selected for the control of the motor. This chip was designed to operate in a stand-alone mode of operation where there are no supporting RAM or ROM chips for the DSP low level program. This

makes the DSP chip nearly impervious to internal crashes and although it is a complex 32 bit device, it has an inherent ruggedness that is not surpassed with any other device. It is well suited to electrically noisy environments where safety is the utmost consideration. This chip also is capable of serving as a component common to a variety of different door control system architectures. This is possible due to the tremendous amount of control range built into the DSP chip 320.

The LM629 is preferred because it lends itself to a motor control design that is almost entirely digital in operation. Because no analog control loops are used (e.g., linear current & tachometer feedback), the IDCU is relatively immune to noise causing position/velocity errors in the operation of the doors.

Figures 4~~, 5B~~ and ~~8C~~5 best illustrate the H-bridge amplifier 330. Driven by the motor current circuitry in the MC-CPLD via pwm and direction signals, the H-bridge amplifier 330 includes optical isolation circuitry 360, level shifting circuitry 362, and field effect transistors (FETs) 364 with which to drive the motor. The lower two FETs are current sensing devices. They provide to the motor current and power monitoring circuitry 326 in the MC-CPLD feedback as to the magnitude of the current in the motor 76. This analog feedback 366 is used only to protect the H-bridge circuitry 330 and the motor 76 during dynamic braking. The IDCU does not use

current feedback to detect obstructions. Circuitry is also employed to protect the components of the H-bridge circuitry 330 and the motor 76 from surge voltages and other adverse electrical influences.

~~During the open stroke, the IDCU also performs an obstruction detection operation. The level of sensitivity can be set differently from that of the close cycle depending upon the importance for shorter cycle times. During the open stroke, the lock members 43 and 122 are mechanically latched up thereby allowing the power to be removed from their respective solenoids. This method extends the life expectancy of the solenoids and also reduce the power consumed by the IDCU.~~

An encoder 368 provides digital feedback to the MC-CPLD 318.

The IDCU also makes use of four limit switches to help qualify the real position of the doors. These switches are best shown in Figures 4 and ~~5A-B~~5. These switches include (1) two door close limit switches (one per door panel) showing the doors are in the closed position 616; (2) two pushback lock switches 58 each indicating that its lock member is partially engaged, i.e., in the pushback-locked state; (3) two full lock switches 56 each indicating that its lock member is fully engaged, i.e., in the fully-locked state. In this state, the full lock switches indicating to the IDCU that the power need no longer be supplied to

the motor 76. Other inputs to the IDCU are push back position switches 340, external and internal emergency door release switches 342 and 344, respectively, and a passenger door hold/open push button switch 346.

The power supply card 400 includes a system breaker (protective circuits) 410, a switching power supply 420 and monitoring circuitry 430.

While the presently preferred embodiment for carrying out the instant invention has been set forth in detail, those persons skilled in the digital circuit art to which this invention pertains will recognize various alternative ways of practicing the invention without departing from the spirit and scope of the patent claims appended hereto.

ABSTRACT

A ~~programmable system and~~passenger transit car such as a rail car including a self-locking memory circuit for a tristate data bus having multiple bit lines. The self-locking circuit is located on a printed circuit board that is directly connected a mother board which, in turn, is directly connected to motors, solenoids and switches which couple considerably more electrical noise onto the data lines and the self-locking circuit than the electrical noise present in conventional environments for self-locking circuits. The circuit includes a non-inverting amplifier chip for connection to one of the bit lines and a resistor having a predetermined electrical resistance connected across the amplifier chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit to reduce the effects of electrical noise on the data bus. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below the upper and lower threshold levels of the self-locking circuit. The tristate data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.